Replacement Claims

WHAT IS CLAIMED IS:

101. (amended) A transistor in a semiconductor device, comprising:

source/drain diffusion regions formed on a semiconductive region of a substrate; and

a transistor gate formed on the semiconductive region between the source/drain diffusion regions, the transistor gate extending in a vertical orientation from the substrate, the transistor gate comprising at least two overlying layers of epitaxial silicon, including an uppermost epitaxial layer;

each epitaxial silicon layer comprising a top surface and insulated sidewalls, and the uppermost epitaxial silicon layer having an insulated top surface.

C Cont'd

102. The transistor of Claim 101, wherein the source/drain diffusion regions are elevated and extend in a vertical orientation from the substrate surface adjacent to the transistor gate.

103. (amended) The transistor of Claim 102, wherein each of the source/drain diffusion regions comprise at least two overlying layers of epitaxial silicon, each epitaxial silicon layer having a top surface, and insulated sidewalls, and an uppermost epitaxial silicon layer having an insulated top surface.

104. (amended) The transistor of Claim 103, wherein the uppermost epitaxial silicon layer of the source/drain diffusion regions comprise a conductivity enhancing dopant.

105. (amended) The transistor of Claim 103, wherein each of the epitaxial silicon layers of the source/drain diffusion regions comprise a conductivity enhancing dopant.

106. (amended) The transistor of Claim 101, wherein each epitaxial silicon layer comprises a faceted top surface.

107. (amended) The transistor of Claim 101, wherein each epitaxial silicon layer has a thickness of about 50 to about 200 nm.

108. The transistor of Claim 101, wherein the transistor is isolated within the substrate by at least one dielectric isolation region formed in the substrate adjacent thereto.

109. The method of Claim 108, wherein the at least one dielectric isolation region is a shallow trench isolation region comprising an oxide.

110. (amended) A transistor in a semiconductor device, comprising:

a transistor gate disposed on a semiconductive region of a substrate; and

elevated source/drain diffusion regions disposed on the semiconductive region adjacent to the transistor gate, and extending in a vertical plane from the substrate;

each of the source/drain diffusion regions comprising at least two overlying layers of epitaxial silicon, including an uppermost epitaxial silicon layer; each epitaxial silicon layer comprising a top surface and insulated sidewalls, and the uppermost epitaxial silicon layer having an insulated top surface.

C1 Cont

111. (amended) The transistor of Claim 110, wherein the source/drain diffusion regions comprise an uppermost epitaxial silicon layer comprising a conductivity enhancing dopant.

112. (amended) The transistor of Claim 110, wherein at least one of the epitaxial silicon layers of the source/drain diffusion regions comprise a conductivity enhancing dopant.

113. (amended) The transistor of Claim 112, wherein at least one of the epitaxial silicon layers comprises a concentration gradient of the dopant.

114. (amended) The transistor of Claim 110, wherein the epitaxial silicon layers comprise a faceted top surface.

Replacement Claims

115. (amended) The transistor of Claim 110, wherein each epitaxial silicon layer has a thickness of about 50 to about 200 nm.

116. (amended) The transistor of Claim 110, wherein the transistor gate is covered by a layer of insulative material and comprises at least two overlying layers of epitaxial silicon.

123. (amended) A transistor in a semiconductor device, comprising:

a transistor gate disposed on a semiconductive region of a substrate; and

an elevated source/drain diffusion region disposed on the substrate adjacent to the transistor gate in a vertical orientation from the substrate; the source/drain diffusion region comprising at least two overlying layers of epitaxial silicon, including an uppermost epitaxial layer; each of the at least two epitaxial silicon layers comprising a top surface and sidewalls, with a layer of an insulative material disposed over the sidewalls; and the uppermost epitaxial layer having a top surface with an overlying layer of an insulative material.

124. (amended) The transistor of Claim 123, wherein at least one of the epitaxial silicon layers of the source/drain diffusion region comprises a conductivity enhancing dopant.

125. (amended) The transistor of Claim 124, wherein the uppermost epitaxial silicon layer of the source/drain diffusion region comprises a conductivity enhancing dopant.

126. (amended) The transistor of Claim 124, wherein at least one of the epitaxial silicon layers comprises a concentration gradient of the dopant.

127. The transistor of Claim 124, wherein the conductivity enhancing dopant comprises a p-type dopant.

128. The transistor of Claim 124, wherein the conductivity enhancing dopant comprises an n-type dopant.

129. (twice amended) A semiconductor structure, comprising:

at least two overlying layers of epitaxial silicon, including an uppermost epitaxial layer; each epitaxial silicon layer comprising a top surface and insulated sidewalls, and the uppermost epitaxial layer having an insulated top surface; the structure disposed on a substrate in a vertical orientation.

130. (amended) The semiconductor structure of Claim 129, wherein each epitaxial silicon layer comprises a top surface defining a facet.

131. (amended) The semiconductor structure of Claim 129, wherein the facet has a (100) plane orientation.

132. (amended) The semiconductor structure of Claim 129, wherein each epitaxial silicon layer has a thickness of up to about 200 nm.

133. (amended) The semiconductor structure of Claim 132, wherein each epitaxial silicon layer has a thickness of about 50 to about 200 nm.

134. (amended) The semiconductor structure of Claim 132, wherein one or more epitaxial silicon layers has a thickness of about 70 to about 100 nm.

135. (amended) The semiconductor structure of Claim 132, wherein each epitaxial silicon layer has a thickness of at least about 10 nm to about 30 nm.

136. The semiconductor structure of Claim 129, being disposed adjacent to a gate or word line.

137. The semiconductor structure of Claim 129, being disposed adjacent to a source/drain region.

138. The semiconductor structure of Claim 137, being a transistor gate.

139. The semiconductor structure of Claim 138, wherein the transistor gate is isolated within the substrate by at least one dielectric isolation region disposed in the substrate adjacent thereto.

140. The semiconductor structure of Claim 129, being a source/drain diffusion region.

CD Cont

141. (amended) The semiconductor structure of Claim 140, wherein the uppermost epitaxial silicon layer comprises a conductivity enhancing dopant.

142. (amended) The semiconductor structure of Claim 140, wherein each of the epitaxial silicon layers comprises a conductivity enhancing dopant.

143. (amended) A semiconductor structure, comprising:

at least two overlying layers of epitaxial silicon, each epitaxial silicon layer comprising a top surface and sidewalls, and insulative material over the sidewalls; an uppermost epitaxial silicon layer of the at least two overlying layers having a top surface with an overlying layer of an insulative material; wherein the structure is disposed on a substrate in a vertical orientation.

144. The semiconductor structure of Claim 143, wherein the insulative layer comprises an oxide film, a nitride film, an oxidized nitride film, or a composite oxide/nitride film.

145. The semiconductor structure of Claim 144, wherein the insulative layer comprises a silicon nitride film.

146. The semiconductor structure of Claim 145, wherein the silicon nitride film has a thickness of about 5 to about 20 nm.

147. The semiconductor structure of Claim 144, wherein the insulative layer comprises a silicon oxide film.

148. The semiconductor structure of Claim 147, wherein the silicon oxide film has a thickness of about 2 to about 5 nm.

149. (amended) A semiconductor structure, comprising:

at least two overlying layers of epitaxial silicon, each epitaxial silicon layer comprising a top surface, sidewalls, and an insulative material over the sidewalls; an uppermost epitaxial layer of the at least two overlying layers having a top surface with an overlying layer of an insulative material; one or more of the epitaxial silicon layers comprising a conductivity enhancing dopant; wherein the structure is disposed on a substrate in a vertical orientation.

150. The semiconductor structure of Claim 149, wherein the conductivity enhancing dopant comprises a p-type dopant.

151. The semiconductor structure of Claim 150, wherein the p-type dopant is selected from the group consisting of diborane, boron trichloride, and boron trifluoride, and combinations thereof.

152. The semiconductor structure of Claim 149, wherein the conductivity enhancing dopant comprises an n-type dopant.

153. The semiconductor structure of Claim 152, wherein the n-type dopant is selected from the group consisting of phosphine, arsine, and combinations thereof.

154. The semiconductor structure of Claim 149, wherein one or more of the epitaxial layers comprises a concentration gradient of the dopant within the epitaxial layer.

155. The semiconductor structure of Claim 154, wherein the concentration gradient comprises a low to high concentration of the dopant within the epitaxial layer, with the high dopant concentration at the top surface of the layer.

156. The semiconductor structure of Claim 129, being a component of a transistor.

157. The semiconductor structure of Claim 156, being a transistor gate.

158. The semiconductor structure of Claim 156, being a source/drain diffusion region.

159. The semiconductor structure of Claim 158, wherein at least one of the epitaxial layers of the source/drain diffusion regions comprises a conductivity enhancing dopant.

160. (amended) The semiconductor structure of Claim 159, wherein at least one of the epitaxial silicon layers of the source/drain diffusion regions comprises a concentration gradient of a conductivity enhancing dopant.

161. The semiconductor structure of Claim 157, wherein the transistor gate is disposed over a drain region disposed in the substrate.

162. The semiconductor structure of Claim 161, the drain region is about 50 nm to about 100 nm wide.

163. (amended) The semiconductor structure of Claim 161, wherein the uppermost epitaxial silicon layer of the transistor gate structure comprises a source region doped with a conductivity enhancing dopant.

164. (amended) The semiconductor structure of Claim 163, wherein the uppermost epitaxial silicon layer is at least about 10 nm thick.

165. The semiconductor structure of Claim 156, wherein the transistor is isolated within the substrate by at least one dielectric isolation region formed in the substrate adjacent thereto.

166. The semiconductor structure of Claim 165, wherein the at least one dielectric isolation region is a shallow trench isolation region comprising an oxide.

167. The semiconductor structure of Claim 143, being a component of a transistor.

Cont

168. The semiconductor structure of Claim 167, being a transistor gate.

169. The semiconductor structure of Claim 167, being a source/drain diffusion region.

170. The semiconductor structure of Claim 149, being a component of a transistor.

171. The semiconductor structure of Claim 170, being a transistor gate.

172. The semiconductor structure of Claim 170, being a source/drain diffusion region.

173. (amended) A semiconductor structure, comprising:

at least two overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer comprising a top surface and insulated sidewalls, and the uppermost epitaxial silicon layer having an insulated top surface; the structure disposed on a substrate in a vertical orientation; the structure being a component of a transistor.

174. The semiconductor structure of Claim 173, being a transistor gate.

175. The semiconductor structure of Claim 173, being a source/drain diffusion region.

176. (amended) A semiconductor structure, comprising:

at least two overlying layers of epitaxial silicon, each epitaxial silicon layer comprising a top surface, sidewalls, and insulative material over the sidewalls; an uppermost epitaxial silicon layer of the at least two overlying layers having a top surface with an overlying layer of an insulative material; the structure disposed on a substrate in a vertical orientation; the structure being a component of a transistor.

177. The semiconductor structure of Claim 176, being a transistor gate.

178. The semiconductor structure of Claim 176, being a source/drain diffusion region.

Cont

179. (amended) A semiconductor structure, comprising:

at least two overlying layers of epitaxial silicon, each epitaxial silicon layer comprising a top surface, sidewalls, and insulative material over the sidewalls; an uppermost epitaxial silicon layer of the at least two overlying epitaxial silicon layers having a top surface with an overlying layer of an insulative material; one or more of the at least two epitaxial silicon layers comprising a conductivity enhancing dopant; the structure disposed on a substrate in a vertical orientation; and the structure being a component of a transistor.

180. The semiconductor structure of Claim 179, being a transistor gate.

181. The semiconductor structure of Claim 179, being a source/drain diffusion region.

182. (amended) A semiconductor device, comprising:

a structure comprising at least two overlying layers of epitaxial silicon, each epitaxial silicon layer comprising a top surface and insulated sidewalls, and an uppermost epitaxial

silicon layer of the at least two overlying epitaxial silicon layers having an insulated top surface; the structure disposed on a substrate in a vertical orientation.

183. The semiconductor device of Claim 182, comprising a transistor.

184. The semiconductor device of Claim 183, wherein the structure comprises a transistor gate.

185. The semiconductor device of Claim 183, wherein the structure comprises a source/drain diffusion region.

186. (amended) A semiconductor device, comprising:

a structure comprising at least two overlying layers of epitaxial silicon, each epitaxial silicon layer comprising a top surface and sidewalls, and insulative material over the sidewalls; an uppermost epitaxial silicon layer of the at least two overlying epitaxial silicon layers having a top surface with an overlying layer of an insulative material; and the structure disposed on a substrate in a vertical orientation.

Cont

187. The semiconductor device of Claim 186, comprising a transistor.

188. The semiconductor device of Claim 187, wherein the structure comprises a transistor gate.

189. The semiconductor device of Claim 187, wherein the structure comprises a source/drain diffusion region.

190. (amended) A semiconductor device, comprising:

a structure comprising at least two overlying layers of epitaxial silicon, each epitaxial silicon layer comprising a top surface and sidewalls, with insulative material over the sidewalls;

an uppermost epitaxial silicon layer of the at least two overlying epitaxial silicon layers having a top surface with an overlying layer of an insulative material; one or more of the at least two epitaxial silicon layers comprising a conductivity enhancing dopant; and the structure disposed on a substrate in a vertical orientation.

C2 Cont'd

191. The semiconductor device of Claim 190, comprising a transistor.

192. The semiconductor device of Claim 191, wherein the structure comprises a transistor gate.

193. The semiconductor device of Claim 191, wherein the structure comprises a source/drain diffusion region.

194. (new) A transistor in a semiconductor device, comprising:

source/drain diffusion regions disposed on a semiconductive region of a substrate; and

a transistor gate disposed on the semiconductive region between the source/drain diffusion regions, the transistor gate comprising two or more overlying layers of epitaxial silicon extending in a vertical orientation from the substrate, each epitaxial silicon layer comprising a top surface and insulated sidewalls; wherein a first epitaxial silicon layer is disposed on the substrate, and a second epitaxial silicon layer is disposed on the top surface of the first epitaxial silicon layer; and an uppermost epitaxial silicon layer of the transistor gate comprises an insulated top surface.

C3 Cont'

195. (new) A transistor in a semiconductor device, comprising:

a transistor gate disposed on a semiconductive region of a substrate; and

an elevated source/drain diffusion region disposed on the substrate adjacent to the transistor gate in a vertical orientation from the substrate; the source/drain diffusion region comprising at least two overlying layers of epitaxial silicon including an uppermost epitaxial layer; each of the at least two epitaxial silicon layers comprising a top surface, sidewalls, and

insulative spacers over the sidewalls; and the uppermost epitaxial layer having a top surface with an overlying layer of an insulative material.

196. (new) A semiconductor structure, comprising:

at least two overlying layers of epitaxial silicon, each of the at least two epitaxial silicon layers having a top surface, sidewalls, and insulative spacers over the sidewalls; an uppermost epitaxial layer having a top surface with an overlying layer of an insulative material; one or more of the at least two epitaxial silicon layers comprising a conductivity enhancing dopant; and the structure disposed on a substrate in a vertical orientation.

197. (new) A semiconductor structure, comprising:

at least two overlying layers of epitaxial silicon, each epitaxial silicon layer comprising a top surface, sidewalls, and insulative material along the sidewalls; an uppermost epitaxial silicon layer of the at least two overlying epitaxial silicon layers having a top surface with an overlying layer of an insulative material; and the structure disposed on a substrate in a vertical orientation.

C3 Cont

198. (new) A semiconductor structure, comprising:

at least two overlying layers of epitaxial silicon, each epitaxial silicon layer comprising a top surface, and insulated sidewalls; an uppermost epitaxial silicon layer of the at least two overlying epitaxial silicon layers having a top surface with an overlying layer of an insulative material; one or more of the epitaxial silicon layers comprising a conductivity enhancing dopant; and the structure disposed on a substrate in a vertical orientation.

199. (new) A semiconductor structure, comprising:

at least two overlying layers of epitaxial silicon, each epitaxial silicon layer having a top surface, sidewalls, and insulative spacers over the sidewalls; an uppermost epitaxial silicon layer having a top surface with an overlying layer of an insulative material; the structure disposed on a substrate in a vertical orientation; the structure being a component of a transistor.

200. (new) A semiconductor structure, comprising:

at least two overlying layers of epitaxial silicon, each epitaxial silicon layer having a top surface, sidewalls, and insulative spacers over the sidewalls; an uppermost epitaxial silicon layer having a top surface with an overlying layer of an insulative material; one or more of the at least two overlying layers of epitaxial silicon comprising a conductivity enhancing dopant; the structure disposed on a substrate in a vertical orientation; and the structure being a component of a transistor.

201. (new) A semiconductor device, comprising:

a structure comprising at least two overlying layers of epitaxial silicon, each epitaxial silicon layer having a top surface and insulated sidewalls; an uppermost epitaxial silicon layer of the at least two overlying epitaxial silicon layers having a top surface with an overlying layer of an insulative material; and the structure disposed on a substrate in a vertical orientation.

C3 Cont

202. (new) A semiconductor device, comprising:

a structure comprising at least two overlying layers of epitaxial silicon, each epitaxial silicon layer comprising a top surface, and sidewalls covered by an insulative material; an uppermost epitaxial silicon layer of the at least two overlying epitaxial silicon layers having a top surface with an overlying layer of an insulative material; one or more of the epitaxial silicon layers comprising a conductivity enhancing dopant; and the structure disposed on a substrate in a vertical orientation.

203. (new) A semiconductor structure disposed on a substrate, the structure formed by a process comprising the steps of:

selectively growing a first epitaxial silicon layer on the substrate; the first epitaxial silicon layer comprising sidewalls and a top surface;

depositing an insulative layer thereover;

removing a portion of the insulative layer to expose the top surface of the first epitaxial silicon layer;

selectively growing a second epitaxial silicon layer on the exposed top surface of the first epitaxial silicon layer, the second epitaxial silicon layer comprising sidewalls and a top surface; and

depositing an insulative material layer thereover.

204. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing a first epitaxial silicon layer on a substrate;

depositing an insulative film layer thereover;

C3 Cont

removing a portion of the insulative film layer to expose the top surface of the first epitaxial layer;

selectively growing a second epitaxial silicon layer on the exposed top surface of the first epitaxial layer;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the second epitaxial layer;

repeating the steps of selectively growing an epitaxial silicon layer, depositing an insulative film layer, and removing a portion of the insulative film layer to form the stacked structure; wherein, upon selectively growing the uppermost epitaxial silicon layer, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon layer.

205. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying layers of epitaxial silicon to form a stacked, vertically oriented structure;

wherein, prior to selectively growing each epitaxial silicon layer, depositing an insulative film over the underlying epitaxial layers, removing a portion of the insulative film to expose the top surface of the preceding epitaxial layer, and selectively growing the epitaxial silicon layer on the exposed top surface of the preceding epitaxial layer; and,

upon selectively growing the uppermost epitaxial silicon layer, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon layer.

C3 Cont

206. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying layers of epitaxial silicon to form a stacked, vertically oriented structure;

wherein, prior to selectively growing each epitaxial silicon layer, depositing an oxide film and removing a portion of the oxide film to expose the top surface of the preceding epitaxial layer, and selectively growing the epitaxial silicon layer on the exposed top surface of the preceding epitaxial layer; and,

upon selectively growing the uppermost epitaxial silicon layer, depositing an oxide film layer thereover, with no subsequent removal of the oxide film layer from the top surface of said uppermost epitaxial silicon layer.

207. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying layers of epitaxial silicon to form a stacked, vertically oriented structure;

wherein, prior to selectively growing each epitaxial silicon layer, depositing a nitride film and removing a portion of the nitride film to expose the top surface of the preceding epitaxial layer, and selectively growing the epitaxial silicon layer on the exposed top surface of the preceding epitaxial layer; and,

C3 Cont

upon selectively growing the uppermost epitaxial silicon layer, depositing a nitride film layer thereover, with no subsequent removal of the nitride film layer from the top surface of said uppermost epitaxial silicon layer.

208. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying layers of epitaxial silicon to form a stacked, vertically oriented structure by heating the substrate to about 450°C to about 950°C., and flowing at least

one silicon precursor gas over the substrate at a rate of about 10 sccm to about 500 sccm, for about 15 seconds to about 30 seconds;

wherein, prior to selectively growing each epitaxial silicon layer, depositing an insulative film over the underlying epitaxial layers, removing a portion of the insulative film to expose the top surface of the preceding epitaxial layer, and selectively growing the epitaxial silicon layer on the exposed top surface of the preceding epitaxial layer; and,

upon selectively growing the uppermost epitaxial silicon layer, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon layer.

209. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

C3 Cont

selectively growing overlying layers of epitaxial silicon to form a stacked, vertically oriented structure by heating the substrate and flowing at least one silicon precursor gas over the substrate at a rate and pressure to provide a growth rate of the epitaxial layer at about 20 nm/minute to about 40 nm/minute;

wherein, prior to selectively growing each epitaxial silicon layer, depositing an insulative film over the underlying epitaxial layers, removing a portion of the insulative film to expose the top surface of the preceding epitaxial layer, and selectively growing the epitaxial silicon layer on the exposed top surface of the preceding epitaxial layer; and,

upon selectively growing the uppermost epitaxial silicon layer, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon layer.

210. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying layers of epitaxial silicon to form a stacked, vertically oriented structure by heating the substrate and flowing at least one silicon precursor gas over the substrate at a rate and pressure to provide a growth rate of the epitaxial layer of less than about 10 nm/minute;

wherein, prior to selectively growing each epitaxial silicon layer, depositing an insulative film over the underlying epitaxial layers, removing a portion of the insulative film to expose the top surface of the preceding epitaxial layer, and selectively growing the epitaxial silicon layer on the exposed top surface of the preceding epitaxial layer; and

upon selectively growing the uppermost epitaxial silicon layer, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon layer.

C3 Cont

211. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying layers of epitaxial silicon to form a stacked, vertically oriented structure;

wherein, prior to selectively growing each epitaxial silicon layer, forming an insulative film over the epitaxial layers by rapid thermal oxidation, removing a portion of the insulative

film to expose the top surface of the preceding epitaxial layer, and selectively growing the epitaxial silicon layer on the exposed top surface of the preceding epitaxial layer; and,

upon selectively growing the uppermost epitaxial silicon layer, forming an insulative film over the epitaxial layers by rapid thermal oxidation, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon layer.

212. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying layers of epitaxial silicon to form a stacked, vertically oriented structure;

C3 Cont

wherein, prior to selectively growing each epitaxial silicon layer, forming an insulative film over the epitaxial layers by rapid thermal nitridation, removing a portion of the insulative film to expose the top surface of the preceding epitaxial layer, and selectively growing the epitaxial silicon layer on the exposed top surface of the preceding epitaxial layer; and,

upon selectively growing the uppermost epitaxial silicon layer, forming an insulative film over the epitaxial layers by rapid thermal nitridation, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon layer.

213. (new) A semiconductor structure disposed on a substrate, the structure formed by a process comprising the steps of:

selectively growing a first epitaxial silicon layer on the substrate; the first epitaxial silicon layer comprising sidewalls and a top surface;

depositing an insulative layer thereover;

removing a portion of the insulative layer to expose the top surface of the first epitaxial silicon layer;

selectively growing a second epitaxial silicon layer on the exposed top surface of the first epitaxial silicon layer while depositing a conductivity enhancing dopant, the second epitaxial silicon layer comprising sidewalls and a top surface; and

depositing an insulative material layer thereover.

214. (new) A semiconductor structure disposed on a substrate, the structure formed by a process comprising the steps of:

selectively growing a first epitaxial silicon layer on the substrate; the first epitaxial silicon layer comprising sidewalls and a top surface;

depositing an insulative layer thereover;

removing a portion of the insulative layer to expose the top surface of the first epitaxial silicon layer;

selectively growing a second epitaxial silicon layer on the exposed top surface of the first epitaxial silicon layer, the second epitaxial silicon layer comprising sidewalls and a top surface;

C3 Cont

doping the second epitaxial layer with a conductivity enhancing dopant by ion implantation, and

depositing an insulative material layer thereover.

215. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying layers of epitaxial silicon to form a stacked, vertically oriented structure by heating the substrate and flowing at least one silicon precursor gas over the substrate at a rate and pressure to provide a growth rate of the epitaxial layer at about 20 nm/minute to about 40 nm/minute, wherein selectively growing at least the uppermost

epitaxial layer comprises flowing the at least one silicon precursor gas with a conductivity enhancing dopant over the substrate; and

prior to selectively growing each epitaxial silicon layer, depositing an insulative film over the underlying epitaxial layers, removing a portion of the insulative film to expose the top surface of the preceding epitaxial layer, and selectively growing the epitaxial silicon layer on the exposed top surface of the preceding epitaxial layer; and,

upon selectively growing the uppermost epitaxial silicon layer, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon layer.

216. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an insulative film disposed on the top surface;

C3 Cont'

the structure formed by a process comprising the steps of:

selectively growing a first epitaxial silicon layer on a substrate;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the first epitaxial layer;

selectively growing a second epitaxial silicon layer on the exposed top surface of the first epitaxial layer;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the second epitaxial layer; and

repeating the steps of selectively growing an epitaxial silicon layer, depositing an insulative film layer, and removing a portion of the insulative film layer to form the stacked structure; and during the step of selectively growing the uppermost epitaxial layer, depositing a

conductivity enhancing dopant to form a concentration of the dopant within the uppermost epitaxial layer;

wherein, upon selectively growing the uppermost epitaxial silicon layer, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon layer.

217. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing a first epitaxial silicon layer on a substrate;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the first epitaxial layer;

C3 Cont

selectively growing a second epitaxial silicon layer on the exposed top surface of the first epitaxial layer;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the second epitaxial layer; and

repeating the steps of selectively growing an epitaxial silicon layer, depositing an insulative film layer, and removing a portion of the insulative film layer to form the stacked structure; and during the step of selectively growing the uppermost epitaxial layer, depositing a conductivity enhancing dopant at a variable rate to provide a concentration gradient of the dopant within the uppermost epitaxial layer;

wherein, upon selectively growing the uppermost epitaxial silicon layer, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon layer.

218. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing a first epitaxial silicon layer on a substrate;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the first epitaxial layer;

selectively growing a second epitaxial silicon layer on the exposed top surface of the first epitaxial layer;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the second epitaxial layer; and

repeating the steps of selectively growing an epitaxial silicon layer, depositing an insulative film layer, and removing a portion of the insulative film layer to form the stacked structure; and during the step of selectively growing the uppermost epitaxial layer, depositing a conductivity enhancing dopant at an increasing rate over time to provide a low to high concentration of the dopant within the uppermost epitaxial layer;

wherein, upon selectively growing the uppermost epitaxial silicon layer, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon layer.

219. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an

insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing a first epitaxial silicon layer on a substrate;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the first epitaxial layer;

selectively growing a second epitaxial silicon layer on the exposed top surface of the first epitaxial layer;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the second epitaxial layer; and

repeating the steps of selectively growing an epitaxial silicon layer, depositing an insulative film layer, and removing a portion of the insulative film layer to form the stacked structure; wherein the uppermost epitaxial layer is selectively grown while doping, and upon selectively growing the uppermost epitaxial silicon layer, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon layer.

220. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing a first epitaxial silicon layer on a substrate;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the first epitaxial layer;

selectively growing a second epitaxial silicon layer on the exposed top surface of the first epitaxial layer;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the second epitaxial layer; and

repeating the steps of selectively growing an epitaxial silicon layer, depositing an insulative film layer, and removing a portion of the insulative film layer to form the stacked structure;

wherein, upon selectively growing the uppermost epitaxial silicon layer, doping the uppermost epitaxial layer with a conductivity enhancing dopant by ion implantation, and depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon layer.

221. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

C3 Cont

selectively growing overlying layers of epitaxial silicon to form a stacked, vertically oriented structure;

wherein, prior to selectively growing each epitaxial silicon layer, forming an insulative film over the epitaxial layers by rapid thermal oxidation, removing a portion of the insulative film to expose the top surface of the preceding epitaxial layer, and selectively growing the epitaxial silicon layer on the exposed top surface of the preceding epitaxial layer; and, during the step of selectively growing the uppermost epitaxial layer, depositing a conductivity enhancing dopant to form a concentration of the dopant within the uppermost epitaxial layer; and

upon selectively growing the uppermost epitaxial silicon layer, forming an insulative film over the epitaxial layers by rapid thermal oxidation, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon layer.

222. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying layers of epitaxial silicon to form a stacked, vertically oriented structure;

wherein, prior to selectively growing each epitaxial silicon layer, forming an insulative film over the epitaxial layers by rapid thermal nitridation, removing a portion of the insulative film to expose the top surface of the preceding epitaxial layer, and selectively growing the epitaxial silicon layer on the exposed top surface of the preceding epitaxial layer; and, during the step of selectively growing the uppermost epitaxial layer, depositing a conductivity enhancing dopant to form a concentration of the dopant within the uppermost epitaxial layer; and

C3 Cont'

upon selectively growing the uppermost epitaxial silicon layer, forming an insulative film over the epitaxial layers by rapid thermal nitridation, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon layer.

223. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an insulative film disposed on the top surface;

the structure formed by a process comprising the steps of:

selectively growing a first epitaxial silicon layer on a substrate;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the first epitaxial layer;

selectively growing a second epitaxial silicon layer on the exposed top surface of the first epitaxial layer;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the second epitaxial layer; and

C3 Cont'd

repeating the steps of selectively growing an epitaxial silicon layer, depositing an insulative film layer, and removing a portion of the insulative film layer to form the stacked structure; and during the step of selectively growing the uppermost epitaxial layer, depositing a conductivity enhancing dopant to form a concentration of the dopant within the uppermost epitaxial layer;

wherein, upon selectively growing the uppermost epitaxial silicon layer, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon layer.